Notice of References Cited

Application/Control No.

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Examiner

Aimee J. Li

Applicant(s)/Patent Under
Reexamination
LINES ET AL.

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	Α	US-5,488,729	01-1996	Vegesna et al.	712/209
*	В	US-5,884,060	03-1999	Vegesna et al.	712/215
*	С	US-5,428,811	06-1995	Hinton et al.	712/23
*	D	US-6,167,503	12-2000	Jouppi, Norman P.	712/23
	E	US-			
	F	US-			
	G	US-			
	Н	US-			
	_	US-			
	J	US-			
	К	US-			
	L	US-			
	М	US-	,		

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	×				
	0					
	Р				, i	
	Q					
	R					
	S					
	Τ					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)					
	U	Bauer, Jerry; Bershteyn, Michael; Kaplan, Ian; and Vyedin, Paul. "A Recongifurable Logic Machine for Fast Event-Driven Simulation". ACM ©1998					
TV TA	V	Ahlgren, D.C.; Dunn, J.; and Jagannathan, B. "SiGe Comes of Age in the Semiconductor Industry". Future Fab Intl. Volume 3 © 08 July 2002. http://www.future-fab.com/documents.asp?grlD=215&d_ID=1329					
	V	Kröning, Daniel. "Design and Evaluation of a RISC Porcessor with a Tomasulo Scheduler". ©January 1999. Chapter 2: The Scheduling Algorithm.					
	×						

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.